CLAIMS

1. A DC-offset correction circuit (I1, Q1), comprising a DC-offset control loop (O1, O2) embodied by:

- a summing device (9-1, 9-2) having a signal path input (10-1, 10-2), a DC control input (11-1, 11-2), and a summing output (12-1, 12-2); and
- an offset determining means (15-1, 15-2) coupled between the summing output (12-1, 12-2) and the DC control input of the summing device (9-1, 9-2); characterised in that

the DC-offset correction circuit (I1, Q1) further comprises a DC blocking circuit (17-1, 17-2) coupled to the summing output (12-1, 12-2) of the summing device (9-1, 9-2) and having a DC blocking output (18-1, 18-2) for providing an offset corrected output signal.

2. The DC-offset correction circuit (I1, Q1) according to claim 1, characterised in that the DC blocking circuit comprises a high pass filter (17-1, 17-2).

3. A receiver (1) comprising the DC-offset correction circuit (I1, Q1) according to claim 1 or claim 2, characterised in that the receiver (1) comprises channel filter means (DFI, DFQ) coupled between the summing device (9-1, 9-2) and the DC blocking circuit (17-1, 17-2).

4. The receiver (1) according to claim 3, characterised in that the channel filter means comprise analog or digital filters (DFI, DFQ), in case of an analog or digital implementation respectively of said channel filter means.

5. The receiver (1) according to one of the claims 3-4, characterised in that the receiver is a quadrature receiver (1).

6. The receiver (1) according to one of the claims 3-5, characterised in that the receiver is a low-IF receiver, or a zero-IF receiver.

7. The receiver (1) according to one of the claims 3-6, characterised in that the receiver is a double conversion receiver (1).

8. The receiver (1) according to one of the claims 3-7, characterised in that the receiver (1) is provided with analog to digital (AD) converters (13-1, 13-2) and/or digital to analog (DA) converters (16-1, 16-2; 20).

9. The receiver (1) according to one of the claims 3-8, characterised in that the receiver (1) is provided with switchable means (3, 5, 7-1, 7-2).

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